We claim:

1. A method for manufacturing a memory cell circuit, which comprises the steps:

providing a body selected from the group consisting of a semiconductor body and a layer of semiconductor material forming the body;

providing a series of layers on the body, the series of layers including a first oxide layer, a memory layer disposed above the first oxide layer and intended for storing charge carriers, and a second oxide layer disposed above the memory layer;

forming an auxiliary layer on top of the series of layers;

removing the auxiliary layer with an exception of a part over a region of an intended channel region so that a remaining part of the auxiliary layer has sufficiently steep edges;

forming spacers on two mutually opposing edges of the auxiliary layer;

using the spacers as masks and introducing a doping material into the body for forming a source region and a drain region

with a channel region disposed between the source region and the drain region;

removing the remaining part of the auxiliary layer;

removing parts of the second oxide layer applied to the memory layer and parts of the memory layer which have been left free by the spacers;

removing the spacers;

forming a dielectric layer which covers at least the channel region and edges of the memory layer; and

applying a conductor track which runs over the channel region.

2. The method according to claim 1, which comprises using the remaining part of the auxiliary layer during an implantation of a doping material for forming lightly doped drain regions and pocket implants and subsequently isotropically re-etching the remaining auxiliary layer.

3. The method according to claim 1, which comprises:

structuring the conductor track so that it runs in a form of a strip over the source region, the channel region and the drain

region, and parts of the memory layer present at a side of the conductor track are removed during the structuring; and

embedding free edges of the memory layer in an oxide.

4. A memory cell circuit, comprising:

a body selected from the group consisting of a semiconductor body and a layer of semiconductor material forming said body;

a source region and a drain region formed as doped regions in said body;

a channel region disposed in said body and separating said drain region from said source region;

a first oxide layer disposed on said body and having a first part in an area over said source region and a second part in an area over said drain region;

a memory layer disposed on said first oxide layer and intended for storing charge carriers, said memory layer disposed over parts of said source region and parts of said drain region but being interrupted over said channel region;

a second oxide layer disposed on said memory layer;

a dielectric layer disposed on said body between said first and second parts of said first oxide layer;

a gate electrode disposed on said dielectric layer and separated from said body by said dielectric layer; and

an oxide embedding free edges of said memory layer, said oxide formed of an equivalent material as said first and second oxide layers.